Electronic Version
Stylesheet Version v1.1.1

Claims

[c1] 1.A memory address decoding method for determining if a given address is located in one of a plurality of sections, each section having a plurality of memory units and each memory unit having a unique corresponding address, the corresponding addresses using the binary system, the method comprising:
building at least one bit-pattern for each section from the corresponding addresses respectively; and
comparing if at least one comparative bit of the given address matches any of the bit-patterns so as to determine that the given address is located in one of the sections based on the comparison.

[c2] 2.The memory address decoding method of claim 1 wherein the sections are a plurality of memory modules.

[c3] 3.The memory address decoding method of claim 1 wherein the sections are a plurality of rank memory arrays and an even number of rank memory arrays of the same size compose a memory module.

[c4] 4.The memory address decoding method of claim 1 wherein at least one bit-pattern is built for each section,

the bit-pattern consisting of all common bits of the corresponding addresses in each section.

[c5] 5.The memory address decoding method of claim 4 wherein if the comparative bits do not completely match all the bit-patterns of any of the sections, the given address is not located in the section.

[c6] 6.The memory address decoding method of claim 4 wherein if the comparative bits of the given address match the bit pattern of one section, the given address is not greater than the largest address in the section.

[c7] 7.The memory address decoding method of claim 6 wherein determining the given address is located in one of the sections based on the comparison comprises searching for the sections which one of its bit-patterns matches the comparative bits, and judging the given address is located in one section which the greatest corresponding address is the smallest.

[c8] 8.The memory address decoding method of claim 1 wherein at least one bit-pattern is built for each section, the bit-patterns consisting of partial common bits of the corresponding addresses in each section.

[c9] 9.The memory address decoding method of claim 8 wherein if the value of the comparative bits of the given

address do not match all bit-patterns of one section, the given address is not located in the section.

[c10] 10.The memory address decoding method of claim 8 wherein if the value of the comparative bits of the given address matches any of bit-pattern of one section, the given address is not greater than the largest address in the section.

[c11] 11.The memory address decoding method of claim 10 wherein determining the given address is located in one of the sections based on the comparison comprises searching for the sections which one of its bit-patterns matches the comparative bits, and judging the given address is located in one section which the greatest corresponding address is the smallest.

[c12] 12.A control circuit of memory address decoding for determining whether a given address is located in one of a plurality of sections, each section having a plurality of memory units and each memory unit having a unique corresponding address, the corresponding addresses using the binary system, the control circuit comprising:
a pattern calculation module for building at least one bit-pattern for each section based on the corresponding addresses;
an access module for receiving the given address; and

a comparing module for sending a plurality of comparison signals after comparing at least one comparative bits of the given address with each bit-pattern provided by the pattern calculation module and both of them matching.

[c13] 13.The control circuit of claim 12, further comprising a logic module responsible for receiving the comparison signals and sending a decoding result for determining the given address is located in one of sections.

[c14] 14.The control circuit of claim 12 wherein the sections are a plurality of memory modules.

[c15] 15.The control circuit of claim 12 wherein the sections are a plurality of rank memory arrays and an even number of rank memory arrays of the same size compose a memory module.

[c16] 16.The control circuit of claim 12 wherein at least one bit-pattern is built for each section in the pattern calculation module, the bit-pattern consisting of all common bits of the corresponding addresses in each section.

[c17] 17.The control circuit of claim 12 wherein at least one bit-pattern is built for each section in the pattern calculation module, the bit-patterns consisting of partial common bits of the corresponding addresses in each

section.

[c18] 18.The control circuit of claim 12 wherein the comparing module comprises a plurality of comparing units, each comparing unit comprising a plurality of NAND gates and one single AND gate, each of the NAND gates having two inputs for respectively receiving one bit of the bit-patterns and one bit of the given address, the inputs of the NAND gate being connected to the outputs of the AND gate and thereby sending out the comparison signals.